Application: 10/553790

Patent Abstract

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File 347:JAPIO Dec 1976-2010/Jun(Updated 100924)
         (c) 2010 JPO & JAPIO
File 350:Derwent WPIX 1963-2010/UD=201068
         (c) 2010 Thomson Reuters



Set     Items   Description
S1      55746   (MONITOR? ? OR MONITORING) (7N) CIRCUIT? ?
S2        154   (ACTIVITY OR ACTIVITIES) (7N) S1
S3     207183   (PROCESS OR PROCESSING) (7N) CIRCUIT? ?
S4     517749   INPUT (5N) SIGNAL? ?
S5     756521   OUTPUT (5N) SIGNAL? ?
S6          2   CLOAK??? (7N) CURRENT
S7     635012   (POWER (5N) SUPPLY) OR PS
S8       7354   CURRENT (7N) DRAWING (7N) CIRCUIT? ?
S9      23568   (ENCRYPT?? OR ENCRYPTION? ?) (7N) KEY? ?
S10       154   S1 AND S2
S11        22   S2 AND S3
S12         7   S11 AND S4:S5
S13         3   (S12 AND PY=1963:2003) OR (S12 AND AY=1963:2003 AND AC=US)
S14         1   S6 NOT S11
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Dialog eLink: Order File History
14/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350: Derwent WPIX

0014831554 *Drawing available*
WPI Acc no: 2005-179244/200519
Related WPI Acc No: 2004-293311; 2006-547817; 2008-B59672; 2010-H14591
Input buffer circuit for use in computer system, has pair of enabling transistors that are turned on when enable signal is high and cloak signal is low, where current from buffer is withheld when clock signal is high
Patent Assignee: COWLES T B (COWL-I); MICRON TECHNOLOGY INC (MICR-N)
Inventor: COWLES T B

Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update	Type
US 20050024931	A1	20050203	US 2002230545	A	20020829	200519	B
			US 2004928049	A	20040827		
US 7049861	B2	20060523	US 2002230545	A	20020829	200635	E
			US 2004928049	A	20040827		

Priority Applications (no., kind, date): US 2002230545 A 20020829; US 2004928049 A 20040827

Patent Details

Patent Number	Kind	Lan	Pgs	Draw	Filing Notes	
US 20050024931	A1	EN	9	4	Division of application	US 2002230545
					Division of patent	US 6801061
US 7049861	B2	EN			Continuation of application	US 2002230545
					Continuation of patent	US 6801061

...**has pair of enabling transistors that are turned on when enable signal is high and cloak signal is low, where current from buffer is withheld when clock signal is high**

Patent Fulltext

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File 348:EUROPEAN PATENTS 1978-201042
         (c) 2010 European Patent Office
File 349:PCT FULLTEXT 1979-2010/UB=20101021|UT=20101014
         (c) 2010 WIPO/Thomson
```

Set	Items	Description
S1	27619	(MONITOR? ? OR MONITORING) (7N) CIRCUIT? ?
S2	313	(ACTIVITY OR ACTIVITIES) (7N) S1
S3	109879	(PROCESS OR PROCESSING) (7N) CIRCUIT? ?
S4	224754	INPUT (5N) SIGNAL? ?
S5	285091	OUTPUT (5N) SIGNAL? ?
S6	7	CLOAK??? (7N) CURRENT
S7	324357	(POWER (5N) SUPPLY) OR PS
S8	1233	CURRENT (7N) DRAWING (7N) CIRCUIT? ?
S9	27082	(ENCRYPT?? OR ENCRYPTION? ?) (7N) KEY? ?
S10	35	S2 (100N) S3
S11	11	S10 (100N) S4:S5
S12	3	(S11 AND PY=1978:2003) OR (S11 AND AY=1978:2003 AND AC=US)
S13	24	S10 NOT S11
S14	16	(S13 AND PY=1978:2003) OR (S13 AND AY=1978:2003 AND AC=US)

No Reference was found

NPL Abstract

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File   8:Ei Compendex(R) 1884-2010/Oct W3
         (c) 2010 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2010/Sep
         (c) 2010 ProQuest Info&Learning
File  65:Inside Conferences 1993-2010/Oct 25
         (c) 2010 BLDSC all rts. reserv.
File   2:INSPEC 1898-2010/Oct W3
         (c) 2010 The IET
File   6:NTIS 1964-2010/Oct W4
         (c) 2010 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2010/Oct W3
         (c) 2010 INIST/CNRS
File  34:SciSearch(R) Cited Ref Sci 1990-2010/Oct W3
         (c) 2010 The Thomson Corp
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 2006 The Thomson Corp
File  99:Wilson Appl. Sci & Tech Abs 1983-2010/Aug
         (c) 2010 The HW Wilson Co.
File 266:FEDRIP 2010/Aug
        Comp & dist by NTIS, Intl Copyright All Rights Res
File  95:TEME-Technology & Management 1989-2010/Sep W2
         (c) 2010 FIZ TECHNIK
File 583:Gale Group Globalbase(TM) 1986-2002/Dec 13
         (c) 2002 Gale/Cengage
File 256:TecTrends 1982-2010/Oct W2
         (c) 2010 Info.Sources Inc. All rights res.
File  56:Computer and Information Systems Abstracts 1966-2010/Sep
         (c) 2010 CSA.
File  60:ANTE: Abstracts in New Tech & Engineer 1966-2010/Sep
         (c) 2010 CSA.
```

Set	Items	Description
S1	23871	(MONITOR? ? OR MONITORING) (7N) CIRCUIT? ?
S2	143	(ACTIVITY OR ACTIVITIES) (7N) S1
S3	157663	(PROCESS OR PROCESSING) (7N) CIRCUIT? ?
S4	134491	INPUT (5N) SIGNAL? ?
S5	142079	OUTPUT (5N) SIGNAL? ?
S6	33	CLOAK??? (7N) CURRENT
S7	593490	(POWER (5N) SUPPLY) OR PS
S8	213	CURRENT (7N) DRAWING (7N) CIRCUIT? ?
S9	16729	(ENCRYPT?? OR ENCRYPTION? ?) (7N) KEY? ?
S10	5	S2 (100N) S3
S11	3	S10 AND PY <= 2003
S12	24	S4:S5 AND S8
S13	1	S12 AND S1
S14	24	S12 NOT S10
S15	3	S14 AND PY <= 2003
S16	3	RD S15 (unique items)
S17	40	(S4 (7N) S5) (30N) S1
S18	26	(S4 (7N) S5) (15N) S1
S19	22	(S4 (7N) S5) (10N) S1
S20	22	S19 NOT (S10 OR S12)

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S21          3    S20 AND PY <= 2003
```

21/5,K/1 (Item 1 from file: 8)
DIALOG(R)File 8: Ei Compendex(R)

0015737379 **E.I. COMPENDEX No:** 2003497765950
Expand Your I/O with the I SUP 2C Bus

Nana, Emmanuel Tomdio
Corresp. Author/Affil: Nana, E.T.: Texas Instruments Inc., Dallas, TX, United States
Corresp. Author email: tomdio@ti.com
Electronic Design (Electron Des) (United States) **2003** 51/25 (75-76)
Publication Date: 20031110
Publisher: Penton Publishing Co.
CODEN: ELODA **ISSN:** 0013-4872
Document Type: Review; Trade Journal **Record Type:** Abstract
Treatment: T; (Theoretical)
Language: English **Summary Language:** English
The method for controlling and **monitoring input** and **output signals** in an integrated **circuit** is discussed. The cost effective method helps in accessing a parallel bus and provides a convenient means of interfacing with different electronic devices. The technique is based on industry standard PCF8574 and PCF8574A devices. The products differ in their inter-integrated circuit (I SUP 2C) addresses.
Descriptors: Computer software; Cost effectiveness; Data transfer; Electric potential; Interfaces (computer); Logic design; Microprocessor chips; Resistors; *Integrated circuits
Identifiers: Bidirectional serial clock (SCL) lines; Bidirectional serial data (SDA) lines
Classification Codes:
911.2 (Industrial Economics)
723.2 (Data Processing)
722.2 (Computer Peripheral Equipment)
721.2 (Logic Elements)
714.2 (Semiconductor Devices & Integrated Circuits)
701.1 (Electricity, Basic Concepts & Phenomena)
704 (Electric Components & Equipment)
2003
The method for controlling and **monitoring input** and **output signals** in an integrated **circuit** is discussed. The cost effective method helps in accessing a parallel bus and provides a ...
Descriptors: